Docket No.: WMP-IFT-808

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

Applic. No.	:	10/694,592	Confirmation No.: 3500
Inventor	:	Eric Pihet	
Filed	:	October 27, 2003	
Title	:	Method for Determining Line Faults in a Bus System and Bus System	
TC/A.U.	:	2114	
Examiner	:	Kamini Patel	
Customer No.	:	24131	

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

BRIEF ON APPEAL

S i r :

This is an appeal from the final rejection in the Office action dated June 7, 2010, finally rejecting claims 12-28, and 30.

Appellants submit this *Brief on Appeal* including payment in the amount of $540.00 to cover the fee for filing the *Brief on Appeal*.

Real Party in Interest:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 12-28 and 30 are rejected and are under appeal. Claims 1-11 and 29 were cancelled.

Status of Amendments:

No claims were amended after the final Office action. A *Notice of Appeal* was filed on August 4, 2010.

Summary of the Claimed Subject Matter:

The subject matter of each independent claim is described in the specification of the instant application. Examples explaining the subject

matter defined in each of the independent claims, referring to the specification by page and line numbers, and to the drawings, are given below.

Independent claim 12 reads as follows:

A method for checking for line faults in a bus system having at least two bus subscribers [page 15, line 13; Fig. 1: 2-5] connected to a data bus [page 15, line 15; Fig. 1: 6] for data communication between the subscribers [page 15, line 13; Fig. 1: 2-5], the data bus [page 15, line 15; Fig. 1: 6] having at least two bus lines [page 15, lines 18-21; Fig. 1: 7, 8], which comprises:

configuring the bus subscribers [page 16, line 31; Fig. 3: 2] with switches [page 17, line 11; Fig. 1B: S21, S22] for placing the subscribers [page 15, line 13; Fig. 1: 2-5] in a recessive state [page 17, line 21] and a dominant state [page 17, line 22];

making available an internal high potential [page 16, line 36; Fig. 3: VCC2] and an internal low potential [page 16, line 37; Fig. 3: GND2] in the bus subscribers [page 16, line 31; Fig. 3: 2];

carrying out a check [page 22, lines 1-4] for a line fault by a bus subscriber [page 15, line 13; Fig. 1: 2-5] only when the bus subscriber

[page 15, line 13; Fig. 1: 2-5] is placed in the dominant state [page 22, lines1-4] by the switches [page 17, line 11; Fig. 1B: S21, S22]; and

carrying out a check for line faults [page 20, line 24] by comparing voltage levels [page 22, line 19; Fig. 3: VCANH] on the bus lines [page 15, lines 18-21; Fig. 1: 7, 8] with threshold values [page 22, line 17; Fig. 3: Vref1+GND_{shift}] related to one of an internal high level [page 22, line 10; Fig. 3; VCC2] and an internal low level [page 22, line 13; Fig. 3; GND2] of the bus subscriber [page 15, line 13; Fig. 1: 2-5].

Independent claim 18 reads as follows:

A bus system, comprising:

a data bus [page 15, line 15; Fig. 1: 6] having at least two bus lines [page 15, lines 18-21; Fig. 1: 7, 8]; and

at least two bus subscribers [page 15, line 13; Fig. 1: 2-5] coupled to said data bus [page 15, line 15; Fig. 1: 6] for serial data transfer of binary data between said bus subscribers [page 15, line 13; Fig. 1: 2-5], at least one of said bus subscribers [page 16, line 31; Fig. 3: 2] having:

at least one control unit [page 15, line 31; Fig. 3, 2b];

switches [page 17, line 11; Fig. 1B: S21, S22] for assuming a switching state placing the one of said bus subscribers [page 16, line 31; Fig. 3: 2] in a dominant state [page 22, lines1-4];

at least one transceiver [page 15, line 36; Fig. 1b: 2a] for at least one of transmission and reception of data signals; and

at least one fault identification device [page 19, lines 7-8; Fig. 3: 27] configured to:

cause the one of said bus subscribers [page 16, line 31; Fig. 3: 2] to be able to assume a recessive state [page 17, line 21] and the dominant state [page 22, lines1-4],

make available an internal high potential [page 22, line 10; Fig. 3; VCC2] and an internal low potential [page 22, line 13; Fig. 3; GND2] in the one of said bus subscribers,

carry out a check for a line fault [page 22, lines 1-4] only when the one of said bus subscribers [page 16, line 31; Fig. 3: 2] is placed in the dominant state [page 22, lines1-4] by said switching state of said switches [page 17, line 11; Fig. 1B: S21, S22], and

carry out a check for line faults [page 20, line 24] by comparing voltage levels on the bus lines [page 15, lines 18-21; Fig. 1: 7, 8] with

threshold values [page 22, line 17; Fig. 3: Vref1+GND_{shift}] related to one of an internal high level [page 22, line 10; Fig. 3; VCC2] and an internal low level [page 22, line 13; Fig. 3; GND2] of the one of said bus subscribers [page 16, line 31; Fig. 3: 2].

Independent claim 30 reads as follows:

A bus system, comprising:

a data bus [page 15, line 15; Fig. 1: 6] having at least two bus lines [page 15, lines 18-21; Fig. 1: 7, 8]; and

at least two bus subscribers [page 15, line 13; Fig. 1: 2-5] coupled to said data bus [page 15, line 15; Fig. 1: 6] for serial data transfer of binary data between said bus subscribers [page 15, line 13; Fig. 1: 2-5], at least one of said bus subscribers [page 16, line 31; Fig. 3: 2] configured to assume a recessive state [page 17, line 21] and a dominant state [page 22, lines1-4] and having:

internal high [page 16, line 36; Fig. 3: VCC2] and low potentials [page 16, line 37; Fig. 3: GND2];

internal high [page 22, line 10; Fig. 3; VCC2] and low levels [page 22, line 13; Fig. 3; GND2];

at least one control unit [page 15, line 31; Fig. 3, 2b];

switches [page 17, line 11; Fig. 1B: S21, S22] for assuming a switching state placing the one of said bus subscribers [page 16, line 31; Fig. 3: 2] in a dominant state [page 22, lines1-4];

at least one transceiver [page 15, line 36; Fig. 1b: 2a] for at least one of transmission and reception of data signals, said transceiver [page 15, line 36; Fig. 1b: 2a] connected to said control unit [page 15, line 31; Fig. 3, 2b]; and

at least one fault identification device [page 19, lines 7-8; Fig. 3: 27] connected to at least said transceiver [page 15, line 36; Fig. 1b: 2a] and carrying out:

a check for a line fault [page 22, lines 1-4] only when the at least one of said bus subscribers [page 16, line 31; Fig. 3: 2] is placed in said dominant state [page 22, lines1-4] by said switching state of said switches [page 17, line 11; Fig. 1B: S21, S22]; and

a check for line faults [page 20, line 24] by comparing voltage levels on said bus lines [page 15, lines 18-21; Fig. 1: 7, 8] with threshold values [page 22, line 17; Fig. 3: $Vref1+GND_{shift}$] related to one of said internal high level [page 22, line 10; Fig. 3; VCC2] and said internal low level [page 22, line 13; Fig. 3; GND2].

Grounds of Rejection to be Reviewed on Appeal

1. Whether or not claims 12-22, 25-28 and 30 are obvious over Eisele et al. (US patent No. 6,034,995, hereinafter referred to as Eisele), in view of Williamson (US patent No. 5,124,990) under 35 U.S.C. § 103(a).

2. Whether or not claim 23 is obvious over Eisele and Williamson in view of Barclay et al. (US patent No. 4,516,248, hereinafter referred to as Barclay) under 35 U.S.C. § 103(a).

3. Whether or not claim 24 is obvious over Eisele and Williamson in view of Baker (U.S. Patent No. 6,535,028) under 35 U.S.C. § 103(a).

Argument:

Claims 12-22, 25-28 and 30 are not obvious over Eisele et al. in view of Williamson

Claim 12 includes a step of" "carrying out a check for a line fault by a bus subscriber only when the bus subscriber is placed in the dominant

state by the switches". The Examiner has recognized that Eisele et al. do not teach such a step. The Examiner has alleged that Williamson teach such a step and that it would have been obvious to have incorporated the step taught in Williamson into the teaching of Eisele et al.

Appellant respectfully believes that when one considers the teachings in the prior art as a whole, as is required, the invention as defined by claim 12 would not have been suggested. Eisele et al. teach a data bus that includes two data lines 11 and 12. All stations 1, 2, 3 or subscribers are connected in parallel to the data lines 11 and 12 such that the data is simultaneously transmitted from one subscriber to all of the other subscribers connected in parallel to the data lines 11, 12. Williamson, however, does not teach a transmission bus in which the data is transmitted simultaneously to all subscribers connected in parallel to the data lines. Williamson teaches a bidirectional ring configuration 500 with a plurality of data bus portions 510AB, 510BC, 510CA located between the subscribers 502 in which data can be transmitted sequentially. The sequential transmission occurs, for example, from one subscriber 502A to the next subscriber 502B and then to the next subscriber 502C along the ring 500 (See Fig. 5).

Williamson places only one segment of the serial data bus 510AB, 510BC, or 510CA in the dominant state in order to check only the segment of the data bus 510AB, 510BC, or 510CA that is in the dominant state (See Fig. 6 and column 4, line 55 through column 5, line 19).

Not only are there differences in topology between the two different types of networks, but there are differences in protocols, and in the general operation of a ring network with respect to a network in which all of the subscribers are connected in parallel to the data bus. Because of these differences, appellant believes that one of ordinary skill in the art concerned with designing a parallel data bus, such as that taught by Eisele et al., would not even refer to a teaching of a ring network, such as that taught by Williamson, where the data is transmitted along the ring from one subscriber to the next subscriber on the ring.

Further, even if one of ordinary skill in the art concerned with designing a parallel data bus, did consider the teaching of Williamson, appellant believes it would not have been obvious to have incorporated the teaching in Williamson into that of Eisele et al. This is the case

because Williamson tests one half of a bidirectional portion of a data bus that is located between the receiver of one subscriber of a ring network and the transmitter of another subscriber of the ring network, and it would not have been obvious to have incorporated that teaching into a parallel data bus, such as, that taught by Eisele et al. The data bus in Eisele et al. does not have discrete portions located only between a particular receiver and a particular transmitter. Rather, the data bus in Eisele et al. is connected to all subscribers. Inventive and creative thought would have been needed to even contemplate applying a feature of a ring network to a parallel data bus.

The invention as defined by claim 12 would not have been suggested when one considers the teachings in the prior art as a whole in order to determine what fairly would have been suggested to one of ordinary skill in the art.

Claim 18 defines a bus with at least one fault identification device configured to carry out a check for a line fault only when the one of said bus subscribers is placed in the dominant state by said switching state of said switches. Claim 30 defines a bus at least one fault identification device connected to at least said transceiver and carrying out: a check

for a line fault only when the at least one of said bus subscribers is placed in said dominant state by said switching state of said switches.

Referring to the limitations of claims 18 and 30 copied above, it is seen that the discussion provided with regard to claim 12 is also applicable to claims 18 and 30. It is believed to be clear that the invention as defined by claim 18 and the invention as defined by claim 30 would not have been suggested.

Claim 23 is not obvious over Eisele et al. and Williamson in view of Barclay et al.

Appellant believes that even if the teaching in Barclay et al. were considered, the invention as defined by claim 23 would not have been suggested for the reasons given above with regard to claim 18 and the teachings in Eisele et al. and Williamson.

Claim 24 is not obvious over Eisele et al. and Williamson in view of Baker

Appellant believes that even if the teaching in Baker were considered, the invention as defined by claim 24 would not have been suggested for the reasons given above with regard to claim 18 and the teachings in Eisele et al. and Williamson.

The honorable Board is therefore respectfully urged to reverse the final rejection of the Primary Examiner.

If an extension of time is required for this submission, petition for extension is herewith made. Any fees due should be charged to Deposit Account No. 12-1099 of Lerner Greenberg Stemer LLP.

Respectfully submitted,

/Mark P. Weichselbaum/
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Claims Appendix:

12. A method for checking for line faults in a bus system having at least two bus subscribers connected to a data bus for data communication between the subscribers, the data bus having at least two bus lines, which comprises:

configuring the bus subscribers with switches for placing the subscribers in a recessive state and a dominant state;

making available an internal high potential and an internal low potential in the bus subscribers;

carrying out a check for a line fault by a bus subscriber only when the bus subscriber is placed in the dominant state by the switches; and

carrying out a check for line faults by comparing voltage levels on the bus lines with threshold values related to one of an internal high level and an internal low level of the bus subscriber.

13. The method according to claim 12, which further comprises:

providing a supply voltage referenced to an internal reference ground potential in the bus subscribers, the threshold values being greater than the supply voltage; and

identifying a fault when one of the voltage levels on the bus lines is greater than the respective threshold value.

14. The method according to claim 13, which further comprises identifying a fault when one of the voltage levels on the bus lines is greater than the respective threshold value during a predetermined number of successive dominant states of the bus subscriber carrying out the fault identification.

15. The method according to claim 12, which further comprises:

comparing the voltage levels on the data lines with one another for detection of transmitted data; and

upon detection of a fault on one of the data lines, carrying out detection of transmitted data by comparing the voltage level on the other one of the data lines with a threshold value related to one of the internal high potential and the internal low potential.

16. The method according to claim 13, which further comprises:

comparing the voltage levels on the data lines with one another for detection of transmitted data; and

upon detection of a fault on one of the data lines, carrying out detection of transmitted data by comparing the voltage level on the other one of the data lines with a threshold value related to one of the internal high potential and the internal low potential.

17. The method according to claim 14, which further comprises:

comparing the voltage levels on the data lines with one another for detection of transmitted data; and

upon detection of a fault on one of the data lines, carrying out detection of transmitted data by comparing the voltage level on the other one of the data lines with a threshold value related to one of the internal high potential and the internal low potential.

18. A bus system, comprising:

a data bus having at least two bus lines; and

at least two bus subscribers coupled to said data bus for serial data transfer of binary data between said bus subscribers, at least one of said bus subscribers having:

at least one control unit;

switches for assuming a switching state placing the one of said bus subscribers in a dominant state;

at least one transceiver for at least one of transmission and reception of data signals; and

at least one fault identification device configured to:

cause the one of said bus subscribers to be able to assume a recessive state and the dominant state,

make available an internal high potential and an internal low potential in the one of said bus subscribers,

carry out a check for a line fault only when the one of said bus subscribers is placed in the dominant state by said switching state of said switches, and

carry out a check for line faults by comparing voltage levels on the bus lines with threshold values related to one of an internal high level and an internal low level of the one of said bus subscribers.

19. The bus system according to claim 18, further comprising at least one fault detection device comparing at least one voltage level on one

of said bus lines with a threshold value related to one of the internal low level and the internal high level and providing a fault signal.

20. The bus system according to claim 19, wherein said at least one fault detection device is:

a first fault detection device comparing a voltage level on one of said data lines with a first threshold value and provision a first fault signal; and

a second fault detection device comparing a voltage level on the other one of said data lines with a second threshold value and providing a second fault signal.

21. The bus system according to claim 20, further comprising a first data detection device for detection of transmitted data, said first data detection device comparing voltage levels on said bus lines and providing a first data signal.

22. The bus system according to claim 21, further comprising:

at least one second data detection device for detection of transmitted data, said second data detection device comparing a

voltage level on at least one of said data lines with at least one threshold value related to the internal low level to provide at least one second data signal; and

a switch switching between said first data signal and said at least one second data signal as a function of said at least one fault signal.

23. The bus system according to claim 18, wherein said data bus serially transmits binary data by duplex signals and is in the form of a differential, two-wire data bus having two bus lines twisted with one another.

24. The bus system according to claim 18, wherein the bus system is a CAN bus system.

25. The bus system according to claim 18, further comprising at least one means for detecting a fault, said fault detecting means comparing at least one voltage level on one of said bus lines with a threshold value related to one of the internal low level and the internal high level and providing a fault signal.

26. The bus system according to claim 25, wherein said at least one fault detection device is:

a first means for detection a fault, said first fault detecting means comparing a voltage level on one of said data lines with a first threshold value and provision a first fault signal; and

a second for detection a fault, said second fault detecting means comparing a voltage level on the other one of said data lines with a second threshold value and providing a second fault signal.

27. The bus system according to claim 26, further comprising a first means for detecting transmitted data, said first data detection means comparing voltage levels on said bus lines and providing a first data signal.

28. The bus system according to claim 27, further comprising:

at least one second means for detecting data comparing a voltage level on at least one of said data lines with at least one threshold value related to the internal low level to provide at least one second data signal; and

a means for switching between said first data signal and said at least one second data signal as a function of said at least one fault signal.

30. A bus system, comprising:

a data bus having at least two bus lines; and

at least two bus subscribers coupled to said data bus for serial data transfer of binary data between said bus subscribers, at least one of said bus subscribers configured to assume a recessive state and a dominant state and having:

internal high and low potentials;

internal high and low levels;

at least one control unit;

switches for assuming a switching state placing the one of said bus subscribers in a dominant state;

at least one transceiver for at least one of transmission and reception of data signals, said transceiver connected to said control unit; and

at least one fault identification device connected to at least said transceiver and carrying out:

a check for a line fault only when the at least one of said bus subscribers is placed in said dominant state by said switching state of said switches; and

a check for line faults by comparing voltage levels on said bus lines with threshold values related to one of said internal high level and said internal low level.

Evidence Appendix:

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or any other evidence has been entered by the Examiner and relied upon by appellant in the appeal.

Related Proceedings Appendix:

No prior or pending appeals, interferences or judicial proceedings are in existence which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this appeal. Accordingly, no copies of decisions rendered by a court or the Board are available.